Reducing The Effects Of The Mounting Substrate On The Performance Of GaAs MMIC Flip Chips

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Abstract

Flip chip technology has been used in electronic equipment for 25 years or more. This is due to the benefits offered by flip chips such as improved interconnect performance, high reliability, and low cost. Increased packaging demands in wireless communications, and military electronics have lead to the use of flip chips for r.f. and microwave components. For instance, GaAs MMIC flip chips at 15 Ghz have been developed. There a few key technology issues which allow the use of flip chip at microwave frequencies. The most important being the use of coplanar transmission lines. The impact of flipping a MMIC chip are examined using finite element simulations and test data is presented for a flipped microwave GaAs MMIC.

1.0 Introduction

Increased packaging demands in both commercial and military electronics have caused significant technology advances in microwave modules. One such advance is the use of flip chip technology for GaAs MMICs (1,2). Although flip chip technology has been used for 25 years or more, until 1987, it had not been applied to MMIC chips (3). The advantages of improved interconnect performance, high reliability, and low cost provided the motivation for applying flip chip to MMICs.

Figure1 is a simplified cross-sectional view of a GaAs flip chip. As can be seen, CPW is used as the transmission line. The purpose of CPW is to eliminate the need for vias to the backside of the chip, confine the fields within the gaps thereby reducing the interactions with the mounting substrate, and allow for the use of full thickness (635 μm) wafers. Unlike microstrip, CPW is capable of very narrow (or wide) transmission lines relatively independent of the thickness of the wafer. Full thickness wafers are high yield in wafer processing and board integration.

In order to use CPW with full thickness wafers, the effects of the mounting substrate need to be quantified. This is due to the fact that the performance of the MMIC can change significantly when it is flipped. That is, the flipped verses unflipped performance can be very different if the fields within the transmission line on the MMIC interact with the mounting substrate. For testability and design reasons, this is undesirable. The unwanted interactions can be minimized by making a few key design choices. The three most significant parameters effecting the interaction are the MMIC transmission line type, the spacing between the flip chip and mounting substrate, and the transition into the chip.

The effects of flipping a GaAs MMIC will be examined. Specifically, this paper will examine transmission line performance, chip to board spacing, and the chip to board transition. The analysis will culminate with test data for a GaAs MMIC LNA comparing flipped verses unflipped performance.

2.0 MMIC Transmission Line Choice

Since the choice of the type of transmission line to use in GaAs flip chips is critical, a comparison between two possible transmission lines will be used to illustrate the. possible problems. If one were to use

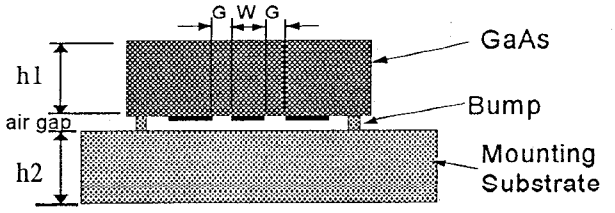

Figure 1. A simplified view of a GaAs flip chip on a mounting substrate

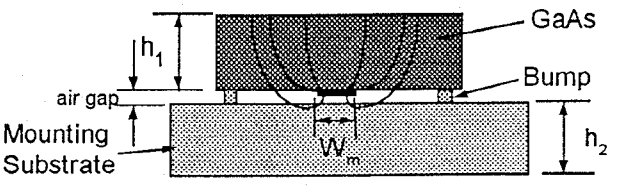

Figure 2. Approximate field distribution for a microstrip flip chip.

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microstrip, for instance, the fields around the transmission line would be similar to what is shown in Figure 2. If a full thickness wafer is used for manufacturability, the line width of the microstrip will be very large. Notice the possibility of significant fringing of the fields into the mounting substrate for the flipped verses unflipped case. The effect on the transmission line impedance is significant. The variational technique was used to simulate this effect. Figure 3 shows the percent change in line impedance for the flipped verses the unflipped case for various line widths. The difference is larger than 5%. This is unacceptable for most applications.

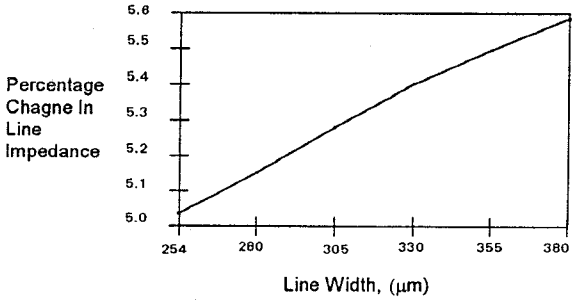

Figure 3. Percentage change in line impedance for a microstrip line on a flip chip (w=varies, h_1=635μm, air gap=100μm, h_2=635 μm).

If, however, one were to choose CPW as the transmission line for the MMIC, the field configuration would be similar to what is shown in Figure 4. Note how the fields are well confined within the gaps on the CPW. This is due to the fact that for full thickness wafers, narrow line widths and gaps are possible for a desired line impedance.

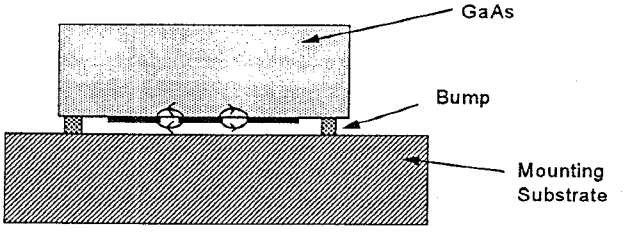

Figure 4. Approximate field distribution for a flipped MMIC using CPW transmission line.

A series of simulations have been done to determine the effect of flipping GaAs MMIC chips which use CPW as the transmission line. The simulations assume full thickness wafers. The purpose of the simulations is to quantify the effect the mounting substrate has on the performance of the chip. The simulations were conducted using the finite element method (4).

The first set of simulations determine the interaction of the chip with the substrate as a function of the dielectric constant of the substrate. The concern is that as the substrate dielectric constant increases, the unwanted stray capacitance may also increase. Degraded performance could result. Since high dielectric constant (ε_r > 8) substrates are desirable for some applications, this effect needed to be understood. Figure 5 demonstrates that these undesired effects do not occur at significant levels. As can be seen, the line

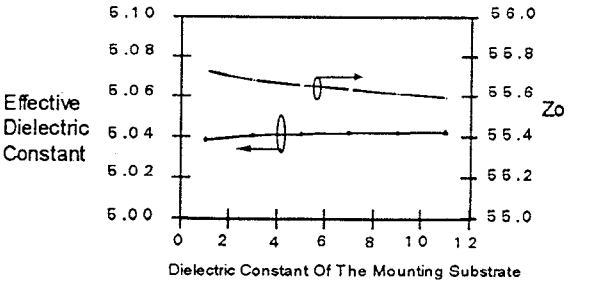

Figure 5. The line impedance and effective dielectric constant are not effected by the mounting substrate even for a dielectric contant up to 11 (w=25.4 μm, G=30.5 μm, h_1=635μm, air gap=100μm, h_2=635 μm).

impedance and effective dielectric constant are unchanged as the mounting substrate dielectric constant is increased. This is due to the fact that the fields in CPW are confined in the gaps and in the GaAs substrate with little fringing into the mounting substrate.

In the next set of simulations the substrate dielectric constant is held constant at ε_r = 8.5 while G is varied. Figure 6 shows the results. As can be seen, rather wide gaps can be used with little effect upon the line impedance when the chips are flipped. In fact, the gaps can be a large as 56 μm with less than 0.3% change in the line impedance when the chips are flipped as compared to unflipped. This is very small compared to the microstrip case. The propagation constant was effected even less.

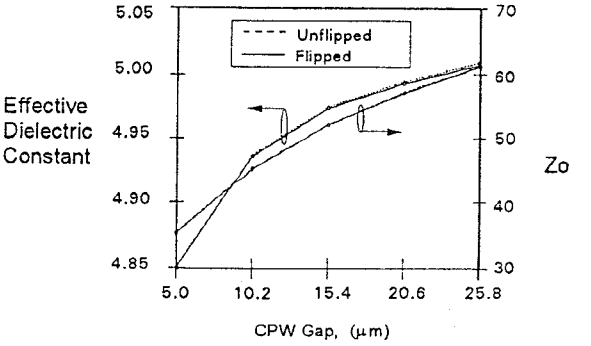

Figure 6. The effective dielectric constant and line impedance are unchanged when the CPW gap is varied (w=14.2 μm, G=varies, h_1=635μm, h_2=635μm, air gap=100μm).

Next, the questions was asked if there is a frequency limit to the use of CPW for GaAs flip chips. Therefore, simulations were run to determine the change in the line impedance and effective dielectric constant for the flipped and unflipped case as a functions of frequency. Figure 7 demonstrates the results. As can be seen, the line impedance is nearly exactly the same for the flipped and unflipped case up to 50 Ghz. In fact, the difference at 50 Ghz is less than 0.53% for the line impedance and 0.035% for the propagation constant. This difference would be very difficult to measure.

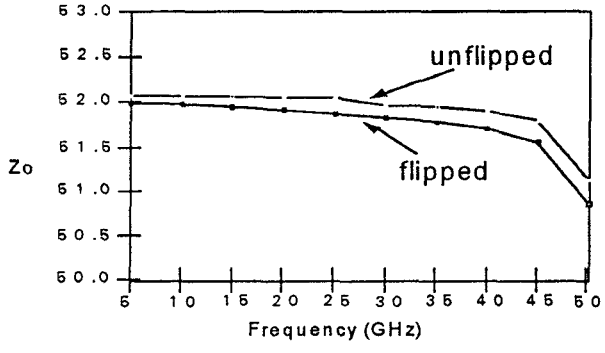

Figure 7. The flipped verses unflipped line impedance of the MMIC agrees extremely well up to 50 Ghz (w=14.2 μm, G=15.42 μm, h_1=635 μm, h_2=635 μm, air gap=100 μm).

3.0 Spacing Between The Chip And The Board

Next, the spacing between the chip and board was examined. As the spacing is reduced, more field fringes into the substrate which reduces the line impedance. Simulations were conducted to determine

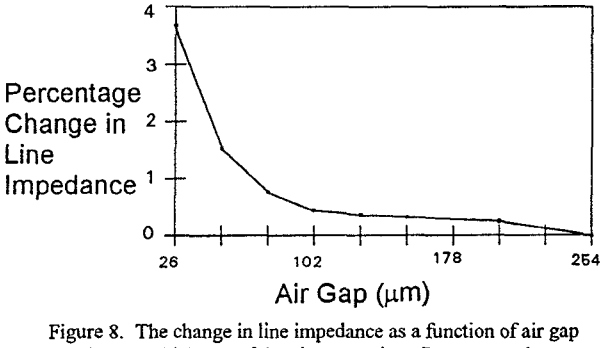

Figure 8. The change in line impedance as a function of air gap determines the thickness of the air gap region. Percentage change as compared to air gap =254 μm (W=76.2 μm, G=50.8 μm, h_1=635 μm, h_2=635 μm).

the optimum spacing between the substrate and the chip. Figure 8 illustrates the results. Base upon the simulations, a spacing of 102 μm was chosen.

4.0 Transition Into The MMIC

Full 3D simulations of the substrate to flip chip transition and interconnect were conducted. This problem has been examined (5) with similar results. Figure 9 shows the simulated structure. The bumps are standard 75 μm high hard bumps with 25 μm high of

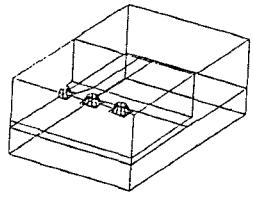

Figure 9. The structure used in the 3D field simulation. The results show very little reflected energy from the transition into the flip chip.

solder. This represents the configuration using standard flip chip manufacturing processes. The critical parameter is the amount of energy reflected from the interconnect to the flip chip. This can be expressed in terms of return loss. The return loss is less than -18dB at 10 Ghz. This result means that existing flip chip bumping and assembly processes could be used, and that the interconnect performance is excellent.

5.0 Test Results

Design guidelines developed as a result of simulations have resulted in a large number of flip chip designs. LNAs, HPAs, drivers, and variable gain amplifiers all using flip chip technology have been developed over the last 7 years. Figure 10 shows a typical example of flipped and unflipped performance of an LNA. Excellent agreement is possible.

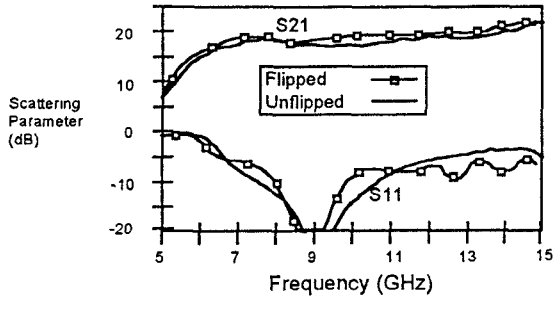

Figure 10. Flipped and unflipped performance of a LNA using CPW transmission line.

6.0 Conclusions

For manufacturability and design reasons, it is desirable to have good agreement between flipped and

unflipped performance of MMIC flip chips. It has been shown that by examining the chip transmission line, the gap between the chip and mounting substrate, and the transition into the chip, design rules can be developed which result in good MMIC test data. Finite element modeling has been presented along with test data for a flipped LNA.

Acknowlegments

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